

**COMPUTER SYSTEM**

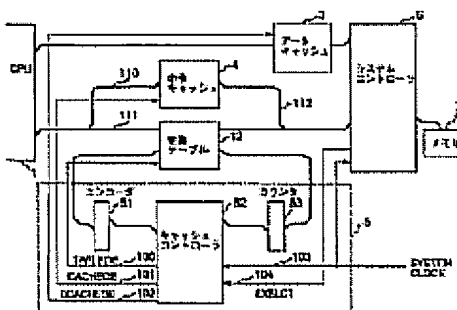
Publication number: JP6266553  
Publication date: 1994-09-22  
Inventor: TSUTSUI MOTOTSUGU  
Applicant: HITACHI LTD  
Classification:  
- International: G06F9/30; G06F9/30; (IPC1-7): G06F9/30  
- European:  
Application number: JP19930056102 19930316  
Priority number(s): JP19930056102 19930316

Report a data error here

**Abstract of JP6266553**

**PURPOSE:**To support a CISC type instruction by an RISC type processor.

**CONSTITUTION:**A conversion table 2 stores the correspondence between the instruction codes that are not supported by a CPU 1 and a string of instruction codes that are supported by a processor and attains a function equivalent to those instruction codes that are not supported by the CPU 1. If the instruction code supplied to the CPU 1 directly from a memory 7 or via an instruction cache 4 is not supported by the CPU 1, a controller 5 successively supplies the instruction codes forming a string of instruction codes stored in a conversion table to the CPU 1 in place of those instruction codes supplied from the memory 7.



Data supplied from the esp@cenet database - Worldwide